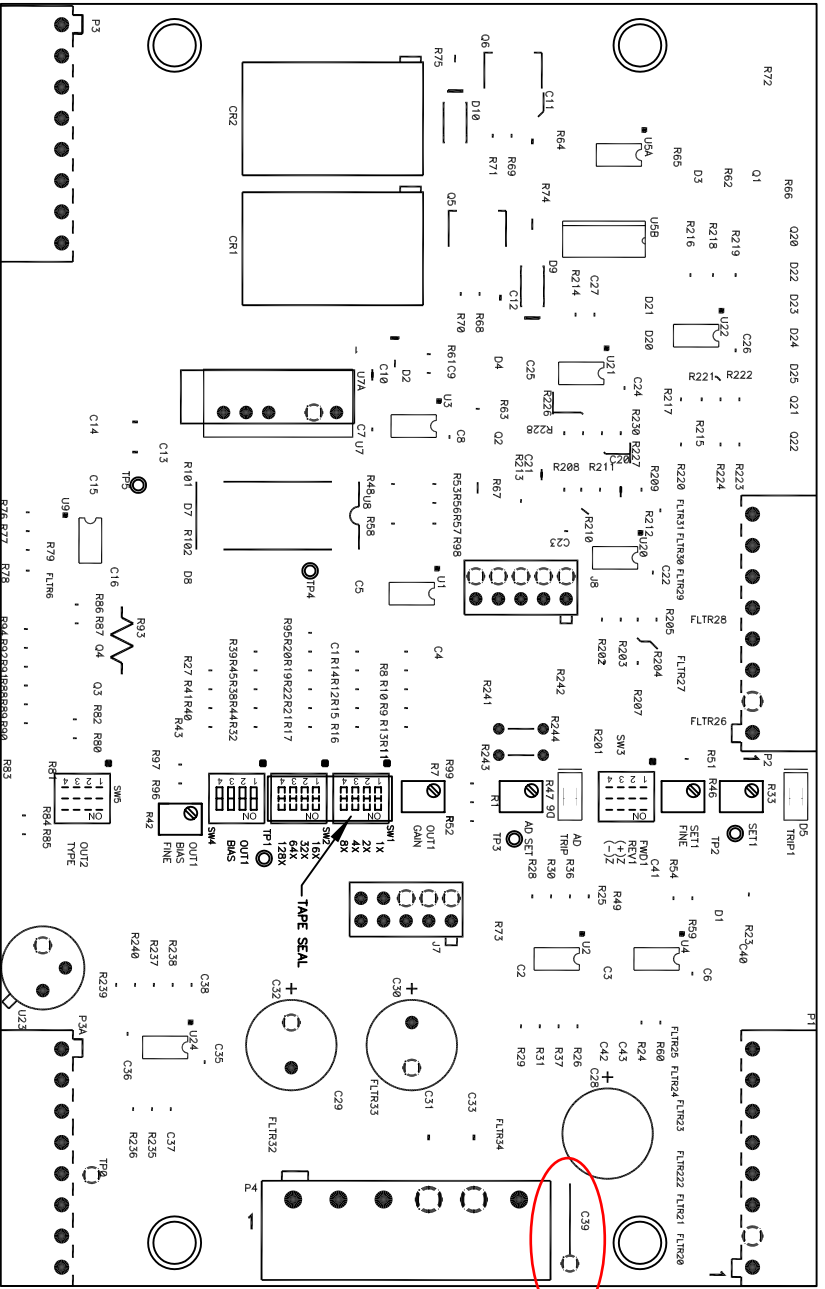


SYM.	REVISION	DRN./DATE	CK'S/DATE
A	CORRECTED OUTPUT 1 BIAS TABLE	RJM 3-18-02	JEM 3-18-02
B	NOTE 3: SWAPPED "OFF" & "ON"	RJM 12-12-02	JEM 12-12-02
C	E-2064: ADD TAPE SEAL	RJM 5-28-03	JEM 5-28-03
D	E-3108: CHG. CR1, CR2, DEL. CR1A, CR2A, R2A, R103, R104	RJM 12-28-04	JEM 12-29-04
E	ECR-1556: CHANGE TO DYNAMP TITLE BLOCK	RJM 2-8-10	



Add 0.1uF 50V ceramic capacitor in parallel with C39. May be added on component (top) or solder (bottom) side of pc board.

T 1 GAIN	OTE 1.)
OPEN	SWITCH
(OFF)	(OFF)
SW1-1	SW1-1
SW1-2	SW1-2
SW1-3	SW1-3
SW1-4	SW1-4
SW2-1	SW2-1
SW2-2	SW2-2
SW2-3	SW2-3
SW1-4	SW1-4

OUTPUT 1 TYPE	
OFFSET	SW5-1&2 SW5-3&4
20mA F.S.	OFF OFF
1V F.S.	ON OFF
10V F.S.	OFF ON

TRIP 1 POLARITY		(see NOTE 3.)	
MODE	SW3-1	SW3-2	
REVERSE	OFF	ON	
FORWARD	ON	OFF	

OUTPUT 1 BIAS (see NOTE 2.)			
OFFSET (mA)	SW4-1	SW4-2	SW4-3 SW4-4
-F.S./0/+F.S.	SW4-1	SW4-2	SW4-3 SW4-4
-20/0/+20	OFF	OFF	OFF ON
-12/+4/+20	ON	OFF	ON OFF
+4/+12/+20	ON	ON	OFF OFF

- NOTE:
- 1.) SW1 & SW2 positions may be opened in any combination for 0X to 128X in 1X increments. (Remove tape seal if necessary.)
 - 2.) OUTPUT 1 BIAS is shown for +20mA current loop output.
1V F.S. or 10V F.S. output types typically use the same SW4 settings as -20/0/+20mA (no bias).
 - 3.) Default for SW3-3 is OFF. Default for SW3-4 is ON.

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B/M NO.(REF.) 045401	THIRD ANGLE PROJECTION	DO NOT SCALE PRINT	TOL. UNLESS OTHERWISE NOTED ±.015	ANG. +1°	TITLE ASSEMBLY LKAT PLUS MAIN PC BOARD	DRN./DATE 9/18-01	APV./DATE 9/18/01	DWG. NO. 75A108586	REV. E
FINISH MATT						CK/D/DATE FEM	SCALE N/A		

DynAmp, LLC GROVE CITY, OHIO